

Appl. No. 10/065,921  
Amdt dated January 20, 2005  
Reply to Office Action dated September 21, 2004

### Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

### Listing of Claims:

1. (currently amended) A method of operating a memory array with reduced noise coupling comprising:

providing a the memory array having a plurality memory cells interconnected by wordlines, bitlines, and platelines, the memory cells of the array are arranged in a plurality of columns, a column comprises a bitline pair having first and second bitlines coupled to a sense amplifier;

performing a memory access to the array, the access selects one of the columns of memory cells; and

providing a plateline pulse to only the selected column while non-selected columns are not provided with the plateline pulse.

2. (original) The method of claim 1 wherein the memory cells are ferroelectric memory cells.

3. (original) The method of claim 2 wherein the memory cells of the array are arranged in an open bitline, a folded bitline, or a series architecture.

4. (original) The method of claim 1 wherein the memory cells of the array are arranged in an open bitline, a folded bitline, or a series architecture.

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5. (currently amended) The method claim 1 wherein ~~unselected~~ non-selected bitlines are set to a defined state.
6. (original) The method of claim 5 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.
7. (original) The method of claim 6 wherein the reference voltage is equal about  $V_{DD}/2$ .
8. (original) The method of claim 7 wherein the non-selected bitlines are floated.
9. (original) The method of claim 8 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
10. (original) The method of claim 7 wherein the plateline pulse is equal to logic 1 or logic 0.
11. (original) The method of claim 10 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
12. (currently amended) The method of claim 8 7 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
13. (original) The method of claim 6 wherein the plateline pulse is equal to logic 1 or logic 0.

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14. (original) The method of claim 13 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
15. (original) The method of claim 13 wherein the non-selected bitlines are floated.
16. (original) The method of claim 15 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
17. (original) The method of claim 5 wherein the plateline pulse is equal to logic 1 or logic 0.
18. (original) The method of claim 17 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
19. (original) The method of claim 17 wherein the non-selected bitlines are floated.
20. (original) The method of claim 19 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
21. (original) The method of claim 5 wherein the non-selected bitlines are floated.
22. (original) The method of claim 6 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

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23. (original) The method of claim 5 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.
24. (currently amended) The method of claim 1 wherein:  
performing the memory access selects x columns of memory cells, where x is a whole number greater than 1, n adjacent columns of each selected column are ~~unselected~~ non-selected, where n is equal to at least 1; and  
providing plateline pulses to the x selected columns.
25. (original) The method of claim 24 wherein 1, some or all x columns are selected for outputting data during the memory access.
26. (original) The method of claim 25 wherein the plateline pulses are equal to logic 1, logic 0, or a combination thereof.
27. (currently amended) The method claim 26 wherein ~~unselected~~ non-selected bitlines are set to a defined state.
28. (original) The method of claim 27 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.
29. (original) The method of claim 28 wherein the non-selected bitlines are floated.
30. (original) The method of claim 27 wherein the non-selected bitlines are floated.

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31. (currently amended) The method claim 25 wherein ~~unselected~~ non-selected bitlines are set to a defined state.
32. (original) The method of claim 31 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.
33. (original) The method of claim 32 wherein the non-selected bitlines are floated.
34. (original) The method of claim 31 wherein the non-selected bitlines are floated.
35. (original) The method of claim 24 wherein the plateline pulses are equal to logic 1, logic 0, or a combination thereof.
36. (currently amended) The method claim 35 wherein ~~unselected~~ non-selected bitlines are set to a defined state.
37. (currently amended) The method of claim 36 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.
38. (currently amended) ~~the~~ The method of claim 37 wherein the non-selected bitlines are floated.
39. (currently amended) ~~the~~ The method of claim 36 wherein the non-selected bitlines are floated.

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40. (currently amended) **[[4he]]** The method claim 24 wherein ~~unselected~~ non-selected bitlines are set to a defined state.

41. (currently amended) **[[4he]]** The method of claim 40 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

42. (currently amended) **[[4he]]** The method of claim 41 wherein the non-selected bitlines are floated.

43. (currently amended) **[[4he]]** The method of claim 40 wherein the non-selected bitlines are floated.